















2023 5 11












# FY2025

	Logic	DRAM	NAND
			
	CPU	DDR5	
	<ul style="list-style-type: none"> <li>§ GAA Nanosheet</li> <li>§ Backside PDN*1</li> </ul>	<ul style="list-style-type: none"> <li>§ EUV</li> <li>§ HKMG*2 CMOS</li> </ul>	<ul style="list-style-type: none"> <li>§</li> <li>§ Multi-tier stack</li> <li>§</li> <li>§</li> </ul>
	<ul style="list-style-type: none"> <li>§</li> <li>§</li> <li>§</li> <li>§</li> </ul>		

FY2024

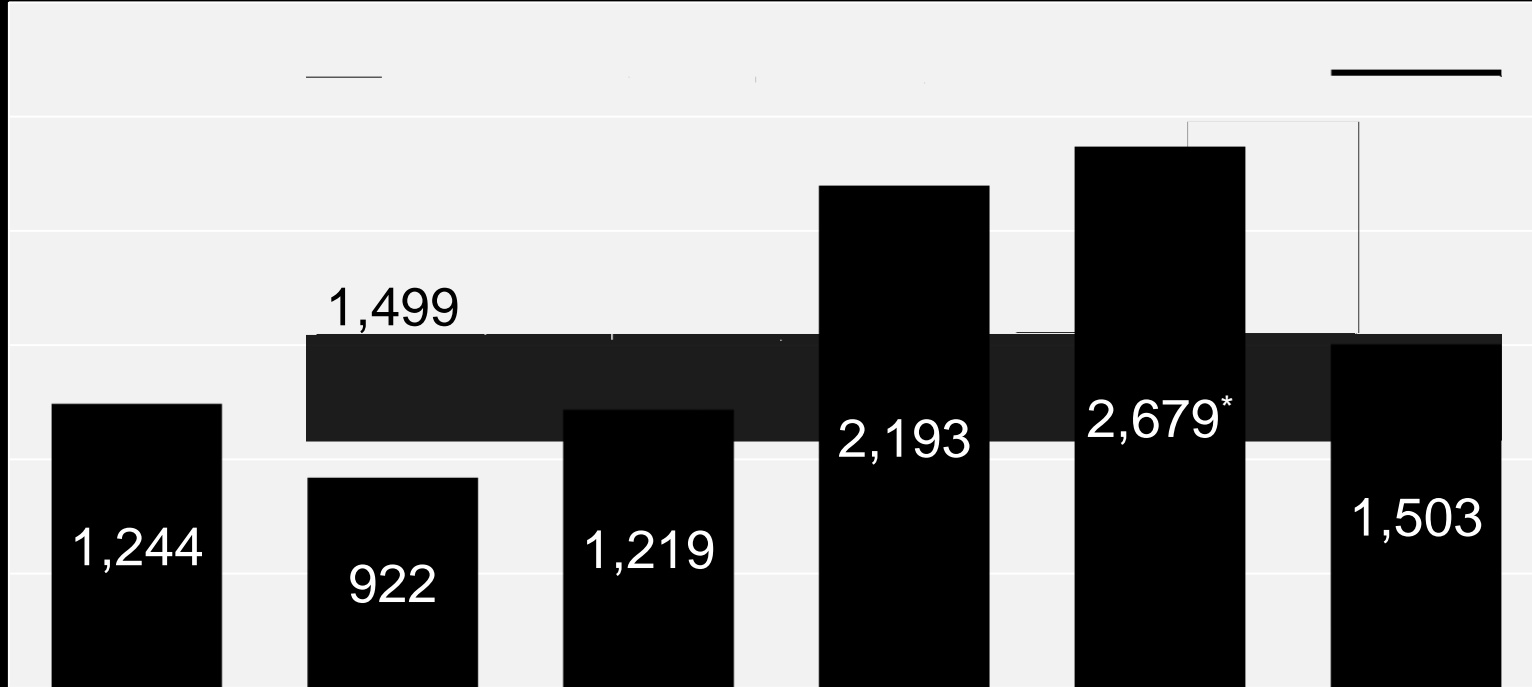






FY2024

















# SPE

